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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,276	01/14/2002	Goro Nakatani	040894-5755	4701
9629	7590	06/27/2008		
MORGAN LEWIS & BOCKIUS LLP			EXAMINER	
1111 PENNSYLVANIA AVENUE NW			IM, JUNGHWA M	
WASHINGTON, DC 20004				
			ART UNIT	PAPER NUMBER
			2811	
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			06/27/2008	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/043,276	NAKATANI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	JUNGHWA M. IM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 28 May 2008.
- 2a) This action is **FINAL**.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1, 3 and 5-13 is/are pending in the application.
  - 4a) Of the above claim(s) 5-7 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,3 and 8-13 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 14 January 2002 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/28/2008 has been entered.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 8 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6410414) in view of Harada et al. (US 6476491), hereinafter Harada.

Regarding claim 1, Fig. 6 of Lee shows semiconductor device comprising:  
a first interconnect layer (102) arranged above a substrate (100) on which a functional semiconductor device is formed (100; active region; col.3, lines 5-10);  
an inter layer dielectric (104) directly covering a portion of top surface and the side surfaces of the first interconnect layer;

a silicon nitride film (106; col.3, line 28) formed so as to cover entirely a top surface of said interlayer dielectric,

a metal interconnect layer (110) covering over said silicon nitride film; and a planarized polyimide (116; col. 5, lines 47-52) which is formed directly on a Surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and an interconnection (114) is connected to the region of the metal interconnect layer.

Fig. 6 of Lee shows substantially the entire claimed structure except the metal interconnect layer (the uppermost metal layer) made of gold and a projection area of the metal interconnect layer connected with a bonding wire is overlapped with said functional semiconductor device. Fig. 7F of Harada shows said metal interconnect layer being consist of gold material (col. 14, lines 38-40); and a planarized polyimide (207; col. 14, line 49) formed on the metal interconnect layer, wherein the polyimide layer is removed at a part of a region of the metal interconnect layer and a projected area of the metal interconnect layer connected to a bond wire (209) is overlapped with the functional semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Harada to the top metal interconnect layer of Lee since a uppermost layer made of gold increases the conductivity and mechanical strength of the interconnection layer, and to have a bond

wire connected to the region of the metal interconnect layer to accommodate the connection of the functional semiconductor device with wires.

Regarding claim 3, Harada discloses that the insulating layers are deposited by plasma CVD method (col. 1, lines 34-35). In addition, “high-density plasma CVD” is a process designation, and would thus not carry patentable weight in this claim drawn to a product. *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 8, Fig. 6 of Lee shows semiconductor device comprising:  
a first interconnect layer (102) arranged above a substrate (100) on which a functional semiconductor region is formed (100);

an inter layer dielectric (104) directly covering a portion of top surface and the side surfaces of the first interconnect layer;

a silicon nitride film (106; col.3, line 28) formed so as to cover entirely a top surface of said interlayer dielectric,

a metal interconnect layer (110) covering over said silicon nitride film; and  
a planarized polyimide (116; col. 5, lines 47-52) which is formed directly on a Surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and an interconnection (114) is connected to the region of the metal interconnect layer.

Fig. 6 of Lee shows substantially the entire claimed structure except the metal interconnect layer (the uppermost metal layer) made of gold, a barrier layer covering the

contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region and a projection area of the metal interconnect layer connected with a bonding wire is overlapped with said functional semiconductor device. Fig. 7F of Harada shows said metal interconnect layer being consist of gold material (col. 14, lines 38-40); and a planarized polyimide (207; col. 14, line 49) formed on the metal interconnect layer, wherein the polyimide layer is removed at a part of a region of the metal interconnect layer and a projected area of the metal interconnect layer connected to a bond wire (209) is overlapped with the functional semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Harada to the top metal interconnect layer of Lee since a uppermost layer made of gold increases the conductivity and mechanical strength of the interconnection layer, and to have a bond wire connected to the region of the metal interconnect layer to accommodate the connection of the functional semiconductor device with wires.

Fig. 7F of Harada shows said metal interconnect layer being consist of gold material (col. 14, lines 38-40), a barrier layer (204a in Fig. 7C) covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region (col. 14, lines 1-10), and a planarized polyimide (207; col. 14, line 49) formed on the metal interconnect layer, wherein the polyimide layer is removed at a part of a region of the metal interconnect layer and a bond wire (209) is connected to the region of the metal interconnect layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the

teachings of Harada to the top metal layer of Lee since a uppermost layer made of gold increases the conductivity and mechanical strength of the interconnection layer, and to have a barrier layer region for improved conductivity, and further to have a bond wire connected to the region of the metal interconnect layer to accommodate the connection of the chip with wires.

Regarding claims 10 and 11, Harada discloses the first interconnect layer consists of aluminum (col. 24, lines 31-32).

Regarding claim 12, Harada discloses the inter layer dielectric consists of USG film (201b, siliconoxide; col. 13, lines 52-55).

Claims 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee/Harada as applied to claim 8 above, and further in view of of Toyosawa et al. (US 6441467), hereinafter Toyosawa.

Regarding claim 9, the combination of Lee/Harada fails to show the barrier layer consists of titanium. Toyosawa disclose that the barrier layer consists of titanium (col. 7, lines 48-50). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Toyosawa to the device of Lee/Harada in order to have the barrier layer consisted of titanium for improved adhesion of the metal.

Regarding claim 13, the combination of Lee/Harada fails to show “the functional semiconductor region further comprises a polysilicon gate isolated from the first interconnect layer by a second dielectric layer, wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the second

dielectric layer. Fig. 1 of Toyosawa shows the functional semiconductor region further comprises a polysilicon gate (3) isolated from the first interconnect layer by a second dielectric layer (10), wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the second dielectric layer. Toyosawa disclose that the barrier layer consists of titanium (col. 7, lines 48-50). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Toyosawa to the device of Lee/Harada in order to have a polysilicon gate isolated from the first interconnect layer by a second dielectric layer, wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the second dielectric layer to operate functionally.

### ***Response to Arguments***

Applicant's arguments filed 5/28/2008 have been fully considered but they are not persuasive.

Applicants argue that "With respect to independent claims 1 and 8, as amended, Applicants respectfully submit that none, of the cited references, whether taken singly or in combination, teaches or suggests the features including at least 'a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and a bonding wire is connected to the region of the metal interconnect layer, wherein a projection area of said region connected with the bonding wire is overlapped with said functional semiconductor device.'" Examiner disagrees. As discussed above in the office action, Fig. 7F of Harada shows a bond wire 209 is connected to the projected

portion of the metal interconnect layer 205 and the projected portion is overlap with the functional semiconductor device 6.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUNGHWA M. IM whose telephone number is (571)272-1655. The examiner can normally be reached on MON.-FRI. 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Junghwa M. Im/  
Examiner, Art Unit 2811

jmi  
6/23/2008

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